Curriculum Vitae, November 2010

TIMOUR T. PALTASHEV

1) CONTACT :

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Legal status: **US citizen**

2) EDUCATION:

Doctor of Science (Computer Engineering) Institute of Fine Mechanics and Optics (IFMO) , October 1994, St.Petersburg, Russian Federation
Ph.D. (Computer Engineering) IFMO, March 1987, Leningrad, USSR
M.Sc. (Electrical Engineering) Kazakhstan Technical University, August 1978, Alma-Ata, USSR

3) WORKBENCH:

Office& Math & Simulation tools: MS Project Manager, MS Office (all components), VISIO, Mapple, Unified Modeling Language UML.

Operating Systems: Unix, MS DOS, all versions of Windows

Hardware design tools: VHDL / Verilog (code development/review and principal bug detection), Synopsys Module Compiler/Express (extensive experience few years ago), Design Compiler, Mentor Graphics ModelSim

Programming tools: C and SystemC (interfaces, algorithms and protocols), C++ (code review and principal bug detection), OpenGL, MS D3D (GPU architecture features), Intel, Motorola ASL (long time ago), MIPS and ARM ASL (teaching MIPS CPU design and SoC design courses in university)

Patent and IP development skills: Expert in patent work and communication with patent attorneys, several own patents were filed, permanent patent research activity in the field of GPU and CPU as well as all patent application preliminary and final review for both HW and SW departments in the company (increased total number more than twice), GPU technical specs and programming manuals development for driver team

Strong academic experience and connections: Long time teaching experience in the fields of computer architecture, computer graphics and embedded digital system, System-on-Chip design. Strong professional connections with graphics and hardware people in UC Davis, Arizona State University, University of Utah, Brigham Young University, Brown University, Tuebingen University (Germany), Lund University (Sweden), Moscow State University.

4) EMPLOYMENT (LAST 10 YEARS):

September 2009 – Present: Full professor in the department of computer engineering of National Research University of Information Technology, Mechanics and Optics, St.Petersburg, Russia
Activity: Pilot project on electronic engineering incubation, SoC technology consulting and PhD candidates' advisory
January 2009 – present : Independent consultant, owner of Gatchina Nanoelectronics LLC (GTnano)
Activity: SoC technology consulting and providing access to TSMC and UMC foundries for Russian fabless companies
January 2001 – January 2009: Graphics Architecture Manager in S3 Graphics Inc., Fremont, CA
Activity: Development of 4 generations (Dx8-9, Dx10, 10.1, Dx11) GPU
January 2003-present: Core faculty member in Northwestern Polytechnic University-Fremont, CA
Activity: Teaching advanced computer architecture and SoC design to graduate students
January 2003-2004: Part time faculty member in California State University-East Bay
Activity: Teaching advanced computer graphics and computer architecture to graduate students
August 2000 – December 2000 Development Manager in architecture group at S3 Inc., Santa Clara, CA:
Activity: Development of various graphics hardware units (architecture and tools
Management of small architecture development team (3 engineers)
January 2000 – July 2000 Senior Graphics Architect in S3 Incorporated, Santa Clara, CA:
Activity: Programmable Geometry and Pixel Engine architecture development;
June 1999 – December 1999 – Consulting Sr. Graphics Architect in S3 Inc., Santa Clara, CA
August 1998- December 1999 Associate Professor in the Department of Electrical and Computer Engineering,

4) PRINCIPAL RESEARCH INTERESTS AND TECHNICAL ACTIVITY:

- SoC with application specific instruction set processors, SoC development tools
- Low power stream architecture for GPU and memory buffers subsystems
- CPU-GPU fusion in System-on-Chip and microarchitecture levels
- SoC Multicore CPU and multiple GPU synchronization protocols and hardware development
- GPGPU application support on GPU architecture/microarchitecture level
- Multiple GPU synchronization and control
- Virtual machine implementation and shader compiler HW support, binary compilation support
- GPU pipeline macro- and micro-synchronization issues
- Dynamic scheduling hardware units for GPU common pool shaders
- Virtual reconfigurable graphics pipeline implementation with common pool of parallel computation units
- Programmable processing units and APIs for 3D Graphics accelerators
- Clock- and bit-accurate computer hardware simulators based on C++ extensions
- Architecture, Hardware Algorithms and VLSI Design for 3D Graphics and Imaging Systems
- Parallel, Pipelined, Multithreaded and Data Flow Multiprocessing for 3D Graphics Accelerators.

5) RESEARCH & DEVELOPMENT EXPERIENCE OVERVIEW:

2006 – 2009 Low power stream GPGPU architecture development, global illumination model mapping to GPU
2005 – present CPU-GPU fusion architecture development, SoC development
2003 – present GPU pipeline internal and external synchronization hardware & software primitives, tools
2001- present Fully programmable parallel graphics architecture with reconfigurable GPU pipeline, algorithms, hardware
1999- present Programmable graphics unified processing units with SIMD, EPIC and MIMD implementation;
1998 - present Behavioral Simulation, Performance Evaluation and clock accurate simulation and performance evaluation of graphics hardware units
1996-1998 Algorithms and Hardware Development for Rational Bezier Surfaces Tessellation, Rasterization and texturing. In cooperation with CS Department of Brigham Young University;
1995-1996 Development of special software tools for creating VRML models of historical center of St.Petersburg for architects and Internet tourism ("Virtual St.Petersburg" Project).
1994-1995 Research on the direct Bezier patches hardware rasterization and shading;
1990-1994 Development of the design technique for 3D multiprocessor graphics accelerators for real-time applications;

6) RESEARCH GRANTS:

July 2009 – September 2010 Russian Federal Government research grant for SoC technology development in National Research University of Information Technology, Mechanics and Optics
August 1999 - July 2000 National Science Foundation, CCR Division, Computer Systems Architecture Program, Grant No. CCR-9908631 “Behavioral Simulation and Performance Evaluation of Imaging System Architecture”
1996-1997 Cooperation in Applied Science and Technology (CAST) Grant, U.S. Academy of Science;
1984-1991 Several soviet military grants (Air Forces, Navy, Aerospace Industry)

7) DISSERTATIONS:

Doctor of Science:

Paltashev, T., “Design of Multiprocessor 3D Graphics Accelerators for Real-Time Rendering Systems“
The Institute of Fine Mechanics and Optics, St.Petersburg, October 1994.

Ph.D.:

Paltashev, T., “Design of Raster Image Generators and Frame Buffers for Graphics Videoterminals”
The Institute of Fine Mechanics and Optics, Leningrad, March 1987.

8) TEACHING EXPERIENCE:

2009 – present "ASIC and ASIP Design: From Algorithms and Instructions to RTL and Chip Layout", "Advanced Microprocessor and SoC architecture" for grads and postgrads in National Research University ITMO
2009 –present "Parallel algorithms and structures", "Computer Architecture" for undergraduate and graduate students in Kazakh-British Technical University, Almaty, Republic of Kazakhstan
2002-present EE504 "Advanced Computer Organization and Design", EE531"Embedded Graphics Software Development for Portable and Handheld Devices", EE615 "System-on-Chip Design" in Northwestern Polytechnic University, Fremont, CA
Winter-Summer 2003 CS-6840 "Computer Graphics" and CS 3430 "Computer Architecture and Algorithms" in Math&CS Dept., California State University, Hayward, CA
Fall 1999 CENG 444 "Computer Networks" and EE 741 "Digital Design" in ECE Dept., SDSM & T;
Spring 1999 CENG 442 "Microprocessor-based Systems Design" and EE 743 "Advanced Digital Systems: An Introduction to Imaging Systems Architecture and VLSI Design" in ECE Dept., South Dakota School of Mines & Technology
Fall 1998 CENG 444 "Computer Networks" and EE 741 "Digital Design" in ECE Dept., SDSM & T;
1996-1997 CS380 "Computer Architecture: A Quantitative Approach" CS Dept., BYU
1994-1996 Fundamentals of Computer Graphics – one semester course; Advanced Computer Graphics – one semester course, Computer Technology Dept., Institute of Fine Mechanics and Optics.

9) PROFESSIONAL VOLUNTEER ACTIVITIES:

2009 -2010 G
2002-2009 ACM SIGGRAPH/EUROGRAPHICS Conference on Graphics Hardware, Program Committee Member;
2004-2005 GRAPHICON'2005 International Conference Co-Chair
1997-present GRAPHICON International Conference Steering Committee Member;
2000 –present Virtual Environment on PC Clusters Workshop Committee Member;
1996 –present Computer Graphics& Geometry Internet Magazine Editorial Board Member
1995-1996 Chairman of GRAPHICON'96 International Conference.
1991-1996 Executive Director of GRAFO Computer Graphics Society;
1994-1995 Chairman of GRAPHICON'95 International Conference;
1994-Present Member of EUROGRAPHICS Association;
1993-Present Member of ACM SIGGRAPH and IEEE CS Professional Associations;
1992-1993 Chairman of GRAPHICON'93 International Conference on Computer Graphics and Visualization;
1990-1992 Member of GRAPHICON'91-92 International Conference Committee;
1990-Present Member of GRAPHICON' International Conference Executive Committee;

10) SELECTED PUBLICATIONS AND PATENTS (from 60+):

1. The Rasterization and Distributed Processing in the Realistic Images Generation // F.Radioelectronics (Russia), 1992, N 11.
2. Analysis of Rasterization Pipeline Using Object Parallelism//Computer Graphics (Russia),1993,V.2, N1.
3. Fast Hardware-Oriented Method of Bezier Patch Shading // Proc. of 4-th International Conference on Computer Graphics and Visualization GRAPHICON'94.- Nizhnij Novgorod, Russia, September 19-25, 1994 and also "Programming Technique" magazine (Russia), 1994, N 3.
4. An Unifying Approach in Fast Hardware-Oriented Rasterization of Curves and Shaded Surfaces // Proceedings of 9-th EUROGRAPHICS Workshop on Graphics Hardware.- Oslo, Norway, Sept.12-13, 1994.
5. New Method of Parametric Curves Rasterization and Its Application for Fast Bezier Patch Shading // Proc. of 5-th Int. Conference GRAPHICON'95.- St.Petersburg, Russia, July 3-7, 1995.
6. Russia: Computer Graphics - Between the Past and the Future // Computer Graphics (ACM SIGGRAPH), May 1996, V.30, N 2.
7. Virtual St.Petersburg for Architects and Internet // Proc. of 5-th Int. Conference GRAPHICON'96 - St.Petersburg, Russia, July 1-5, 1996.
8. One More Approach to Parametric Curves Rasterization and Its Application for Fast Bezier Patch Shading // Proc. of WSCG'97 The Fifth International Conference in Central Europe on Computer Graphics and Visualization, Czech Republic, February 10-14, 1997.

9. Visual Computing Architecture Model Implementation with OpenGL // Proc. of 3-rd IASTED International Conference "Software Engineering and Applications", October 6-8, 1999, Scottsdale, Arizona.

10. Simulation of Hardware Support for OpenGL Graphics Architecture // International Symposium on Information Technology: Coding and Computing (ITCC 2000), Sponsored by IEEE Computer Society, March 27-29, 2000, Las Vegas, Nevada.

11. GOALI: Behavioral Simulation and Performance Evaluation of Imaging System Architecture.// Timour Paltashev, SD School of Mines & Technology, Konstantine Iourcha and Derek Gladding, S3 Incorporated. Technical Report to NSF CISE CSA, Award # 9908631, 2001.

Patents:

1. SU 1665341 - 1991-07-23 “CIRCLE INTERPOLATOR”
2. US 7,737,983 “GPU pipeline multiple level synchronization controller processor and method”
3. US 7,675,521 “Method and apparatus for triangle rasterization with clipping and wire-frame mode support”
4. US 7,659,899 “System and method to manage data processing stages of a logical graphics pipeline”
5. US 7,659,898 “Multi-execution resource graphics processor”
6. US 7,583,268 “Graphics pipeline precise interrupt method and apparatus”
7. US 7,580,040 “Interruptible GPU and method for processing multiple contexts and runlists”
8. US 7,551,174 “Method and apparatus for triangle rasterization with clipping and wire-frame mode support”
9. US7,545,381 “Interruptible GPU and method for context saving and restoring”
10. US 7,284,113 “Synchronous periodical orthogonal data converter”
11. US 7,246,218 “Systems for increasing register addressing space in instruction-width limited processors”
12. US 7,202,872 “Apparatus for compressing data in a bit stream or bit pattern”
13. US 7,159,003 “Method and apparatus for generating sign-digit format of sum of two numbers”
14. US 7,158,143 “Fast algorithm for anisotropic texture sampling”
15. US 7,146,486 “SIMD processor with scalar arithmetic logic units”
16. US 7,098,924 “Method and programmable device for triangle interpolation in homogeneous space”

Published patent applications in pre-grant status:

1. US20100115249 “Support of a Plurality of Graphic Processing Units”
2. US20100110089 “Multiple GPU Context Synchronization Using Barrier Type Primitives”
3. US20100110083 “Metaprocessor for GPU Control and Synchronization in a Multiprocessor Environment”
4. US 20090189909 “Graphics Processor having Unified Cache System”
5. US 20090189896 “Graphics Processor having Unified Shader Unit”
6. US 20090182948 “Caching Method and Apparatus for a Vertex Shader and Geometry Shader”
7. US 20080282034 “Memory Subsystem having a Multipurpose Cache for a Stream Graphics Multiprocessor”
8. US 20080158252 “Method and Apparatus for Triangle Rasterization with Clipping and Wire-Frame Mode Support”
9. US 20070285417 “System and Method for Memory Bandwidth Compressor”
10. US 20070186082 “Stream Processor with Variable Single Instruction Multiple Data (SIMD) Factor and Common Special Function”
11. US 20070185953 “Dual Mode Floating Point Multiply Accumulate Unit”
12. US 20070103476 “Interruptible GPU and method for context saving and restoring”
13. US 20070103475 “Interruptible GPU and method for processing multiple contexts and runlists”
14. US 20070103474 “Graphics pipeline precise interrupt method and apparatus”
15. US 20070091102 “GPU Pipeline Multiple Level Synchronization Controller Processor and Method”
16. US 20070091100 “GPU Pipeline Synchronization and Control System and Method”

17. US 20070030280 “Global spreader and method for a parallel graphics processor”
18. US 20070030279 “System and method to manage data processing stages of a logical graphics pipeline”
19. US 20070030278 “Multi-execution resource graphics processor”
20. US 20070030277 “Method for processing vertex, triangle, and pixel graphics data packets”
21. US 20050134603 “Method and apparatus for triangle rasterization with clipping and wire-frame mode support”
22. US 20050093872 “Method for compressing data in a bit stream or bit pattern”

Japanese, Taiwanese and Chinese derivative patents are not listed.

11) REFERENCES:

Zhores Alferov (VP of RAS, Nobel Prize’2000 in Physics) E.mail: zhores.alferov@mail.ioffe.ru
Professor Boris Babayan (Intel Fellow) E.mail: boris.a.babayan@intel.com
Professor George Hsieh (NPU President) E.mail: georgeh@npu.edu
Konstantine Iourcha (AMD/ATI Research) E-mail: Konstantine.Iourcha@amd.com
Professor Michael Batchelder (SDSM&T) E-mail: michael.batchelder@sdsmt.edu
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(University of Tuebingen, Germany)
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Professor Andries van Dam (Brown University) E-mail: avd@cs.brown.edu
Professor Thomas Sederberg (Brigham Young University) E-mail: tom@byu.edu
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